Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 5 and 6 as follows:-

Listing of Claims:

1-3. (Cancelled)

4. (Previously Presented) A method comprising:

counting clock pulses between two signal transitions of a data stream including pulse widths of a first length and pulse widths of a second length to generate a width value;

comparing the width value with a median pulse width value corresponding to a length between the first length and the second length, the median pulse width value based in part on a previously demodulated pulse width;

outputting a digital signal indicative of the comparison; and

generating a revised median pulse width value using the width value in part by dividing the width value by a first factor to generate a divided value, selecting either the divided value or the width value as a minimum pulse width based in part on the digital signal output, and multiplying the minimum pulse width by a second factor to generate the median pulse width value.

5. (Currently Amended) The method according to claim ~~1~~ 4 wherein the second length is twice as long as the first length, the first factor equal to two, and the second factor equal to 1.5.

6. (Currently Amended) The method according to claim ~~1~~ 4 wherein the act of selecting either the divided value or the width value is performed by a multiplexor, the method further comprising clocking the multiplexor using the digital signal output.

7. (Previously Presented) The method according to claim 6 further comprising filtering the output of the multiplexor.

8. (Previously Presented) The method according to claim 7 further comprising clocking a filter used to perform the act of filtering with a delayed signal based on at least one of the signal transitions.

9. (Previously Presented) An apparatus comprising:

a counter configured to count clock periods between two signal transitions in a data stream including pulse widths of a first length and pulse widths of a second length, the counter configured to output a width value corresponding to a number of clock periods between the two signal transitions;

a comparator configured to receive the width value and compare the width value with a median pulse width and output a digital signal based on the comparison, the median pulse width based in part on a width between two previous transitions of the data stream;

a divider configured to divide the width value by a first factor;

a multiplexor configured to receive the width value, the divided width value, and the output digital signal, the multiplexor configured to output either the width value or the divided width value based in part on the output digital signal; and

a multiplier configured to receive either the width value or the divided width value output by the multiplexor and multiply the received signal by a second factor to generate a revised median pulse width.

10. (Previously Presented) The apparatus according to claim 9 wherein the second length is twice as long as the first length, the first factor equal to two, and the second factor equal to 1.5.

11. (Previously Presented) The apparatus according to claim 9 further comprising a filter coupled to the multiplexor and the multiplier, the filter configured to filter the multiplexor output.

12. (Previously Presented) The apparatus according to claim 11 wherein the filter is configured to receive a delayed signal based in part on at least one of the signal transitions, the filter configured to filter the multiplexor output responsive to the delayed signal.

13. (Previously Presented) The apparatus according to claim 12 further comprising:

an edge detector configured to receive the pulse-width modulated data stream and detect the two signal transitions;

a delay element coupled to the edge detector and configured to generate the delayed signal based on detection of the at least one of the signal transitions.

14. (Previously Presented) The apparatus according to claim 13 further comprising a latch coupled to the counter, the latch configured to receive an indication of a detected signal transition from the edge detector and, responsive to the indication, output the number of clock periods between two data periods to the divider and the multiplexor.

15. (Previously Presented) The apparatus according to claim 9 further comprising a clock oscillator coupled to the counter, the clock oscillator configured to generate the clock cycles.